REMARKS

Claims 1-82 are pending in the application. Claims 1-82 have been rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1-64 of U.S. Patent No. 6,324,623. The Applicant wishes to place this rejection in abeyance until the claims are otherwise allowable.

Claims 1-82 have been rejected under 35 U.S.C. §103 (a) as being deemed unpatentable over Potter et al. (U.S. Patent No. 5,924,093) in view of Poulsen et al. (U.S. Patent No. 5,812,852) and further in view of Hagersten et al. (U.S. Patent No. 5,889,138). Before discussing the cited references however, a brief review of the Applicant's disclosure may be helpful.

A public memory structure is utilized to store data that is shareable between a plurality of users in a multi-threaded computing environment. A memory area on a server shared by a plurality of data accessors is used to store both public, shareable data and private, non-shareable data without having to negotiate ownership. Consequently, there are public and private pages stored in common memory. The private pages are those that are modifiable by a user and the public pages are those that are only readable, although by a plurality of users.

A particular method facilitates simultaneous analysis of data in multiple sessions in a computer. First, data is retrieved from storage into public blocks of a common memory space that is shared by a plurality of user sessions. These public blocks store data for global read-only access by a plurality of user sessions; that is, data in the public blocks is not modifiable by the user sessions. Second, public blocks of data are selectively copied into private blocks of the common memory space. Each private block stores data for private modification (read and write access) by a single user session.

Upon read access to a data item by a user session, the data item is read, if present, from a private block accessible by the user session. If the data item is not present in a private block accessible by the user session, the data item is read from a public block. Upon write access to a data item by the user session, the data item is written to a private block, if present, accessible by the user session. If the private block is not already present, then data is copied from a public to a private block for access by the user session. Any modification to the private block by the user

session is not communicated to the other user sessions. In other words, the claimed invention does not maintain a coherent cache.

Turning to the cited references, the Office is directed to the amendment filed on February 27, 2004 for a discussion of Potter and Poulsen. Newly cited reference, Hagersten discusses maintaining internode and intranode coherency in a multiprocessor computer system having a distributed shared memory architecture. The multiprocessor computer system includes a plurality of SMP nodes each having a local memory. The local memories form a distributed shared memory system. (*See* Fig. 1, memory 22, SMP nodes 12A-D; Col. 8, l. 52-65.)

Hagersten's discussion of a distributed shared memory architecture does not teach or suggest the Applicant's claimed " plurality of memory blocks in the common system memory in the computer shared by the plurality of data accessors". In contrast, Hagersten's distributed shared memory is formed by combining local memory in separate SMP nodes in a multiprocessing system. The SMP nodes communicate over a network and access to a location in the distributed shared memory that is mapped to a local memory on another node requires one or more transactions over the network. (*See* Fig. 1, network 14, SMP nodes 12A-12D, memory 22.)

The cited references separately or in combination do not suggest the need for assigning **a non-modifiable** global view of the first memory block to a first data accessor and a second data accessor, or the need for copying the data from the first memory block to a second memory block in response to a request by the second accessor to modify the first memory block. In contrast, Poulsen merely discusses a **modifiable** global object for the serial thread and a **modifiable** copy of the global object for each of the other threads. Potter discusses a plurality of nodes (computers) in a parallel processing computer system, with each node having its own memory which is **modifiable** only by the respective node. Hagersten merely discusses a plurality of nodes each having its own local memory, the local memories forming a distributed shared memory that stores data that is **modifiable** by any of the nodes.

In contrast to the cited references, the Applicant claims (in Claims 1, 14, 21, 39, 51, 63 and 75) a system that assigns **a non-modifiable global view** of a first memory block to a first and second data accessor in the computer. As claimed, a single non-modifiable global view of data is provided to a plurality of data accessors for global read-only access. In response to a request from the second data accessor to modify the non-modifiable global view of the first

memory block, the data stored in the first memory block is copied to a second memory block and a modifiable private view of that second memory block is assigned to the second data accessor. (*See* Specification, Page 9, lines 9-13.) As claimed, a private, modifiable view of the data, for private modification (read and write access) by a single user session, is assigned to a data accessor in response to a request from the data accessor to modify the data.

The cited references separately or in combination do not teach or suggest at least the Applicant's claimed "assigning a modifiable private view of the second memory block data to the second data accessor in the computer so that a modification to the second memory block data by the second data accessor is not communicated to the first data accessor. Potter is directed to a parallel processing computer system with an array of individual computers (nodes) in which modifications made in local memory in non-co-ordinator nodes **are communicated** to the co-ordinator node. Poulsen discusses the use of copy-out to **communicate** changes in the modifiable copies to the global object. In the cache coherent multiprocessing computer system discussed by Hagersten modifications to local memory in each node **are communicated** in order to maintain coherency in the distributed shared memory. In contrast, in the Applicant's disclosed invention a modification to a modifiable private view **is not communicated**. That is, the Applicant's claimed invention does not maintain a coherent cache.

Furthermore, the Applicant submits that Potter and Poulsen are not properly combinable. Potter's global data structure on a coordinator node stores ordered entries associated with the results stored in local memory in the other nodes. There is no sharing of results between nodes, for example from node B to node D. (*See* Fig. 1) Potter therefore would not motivate one of ordinary skill in the art to add a private view of the global data structure, because each local node stores its own node local data in a private local buffer. Without that motivation, one of ordinary skill would not have combined Potter and Poulsen. Any such combination would be with the aid of hindsight using the Applicant's teachings. Furthermore, Hagersten's implementation of a global coherency protocol teaches away from the Applicant's claimed invention which does not maintain a coherent cache.

Patentably distinguishing claim language of independent Claims 1 and 51 reads, in pertinent part:

storing data in a first memory block in the common system memory of the computer, the plurality of memory blocks in the common system memory shared by the plurality of data accessors;

assigning a **non-modifiable global view** of the first memory block data to a first data accessor and a second data accessor in the computer;

in response to a request by the second data accessor to modify the first memory block, copying the data from the first memory block to a second memory block without regard to the existence of the data in any other memory block; and

assigning **a modifiable private view** of the second memory block data to the second data accessor in the computer so that a modification to the second memory block data by the second data accessor is **not communicated** to the first data accessor.

(*See also* Independent Claim 28.)

In addition, patentably distinguishable claim language of independent Claims 14 and 63 reads, in pertinent part:

. . . public blocks storing data therein for **global read-only access** by a plurality of user accessors;

in response to receiving requests from user accessors to modify public blocks, copying . . . without regard to the existence of the data by any other memory blocks;

. . . upon write access to the data item by the user accessor, writing the data item to a private block **without communicating** any modification to the private block to another user accessor.

(*See also* Independent Claim 39.)

The allowance of dependent claims follow from the base claims. Claims 2-13 are dependent on Claim 1; Claims 15-27 are dependent on Claim 14; Claims 29-38 are dependent on Claim 28; Claims 40-50 are dependent on Claim 39; Claims 52-62 are dependent on Claim 51; Claims 38-43, 48, and 79-82 are dependent on Claim 37; Claims 63-74 are dependent on Claim 63, and Claims 76-82 are dependent on Claim 75 respectively and thus include this limitation over the prior art. Accordingly, the present invention as now claimed is not suggested by the cited art. Reconsideration of the rejections under 35 U.S.C. §103 (a) is respectively requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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